An Efficient Baugh-WooleyArchitecture forBothSigned & Unsigned Multiplication

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Abstract:

This project presents an efficient implementation of a high speed multiplier using the shift and adds method of Baugh-Wooley Multiplier. This parallel multiplier useslesser adders and lesser iterative steps. As a result of which they occupy lesser space as compared to the serial multiplier. This is very important criteria because in the fabrication of chips and high performance system requires components which are as small as possible. Experimental result demonstrate that the proposed circuit not only improves the accurate performance but also reduces the hardware complexity and also less power consumption that is dynamic power of 15.3mW and maximum clock period of 3.912ns is required which is very efficient as compared to the reference paper.

Keywords:
Baugh-Wooley Multiplier, Pipeline resister, PowerEfficient, Carry Save Adder.

1 Introduction

Multiplication involves 2 basic operations: the generation of the partial product and their accumulation [5].Therefore, there are Possible ways to speed up themultiplication: reduces the complexity, and as a result reduces the time needed to accumulate the partial products .Both solutions can be applied simultaneously.

Baugh-WooleyTwo's Compliment Signed Multiplier:Two'sCompliments is the most popular method in representing signed integers in Computer sciences.It is also an operation of negation(Converting positive to negative numbers or vice –versa) in computers which represent negative numbers using two's compliments.Its use is so wide today because it does not require the addition and subtraction circuitry to examine the signs of the operands to determine whether to add or subtract. Two's compliment and one's complimentrepresentations are commonly used since arithmetic units are simpler to design.Fig 1 shows Two's compliment and one's complimentrepresentations.

+N	Positive Integers	-N	Negative Integers		
			Sign & Magnitude	2's Complement	1's Complement
+0	0000	-0	1000	----	1111
+1	0001	-1	1001	1111	1110
+2	0010	-2	1010	1110	1101
+3	0011	-3	1011	1101	1100
+4	0100	-4	1100	1100	1011
+5	0101	-5	1101	1011	1010
+6	0110	-6	1110	1010	1001
+7	0111	-7	1111	1001	1000
+8	----	-8	----	1000	----

FIG1: Two's compliment & one's compliment representation

Baugh-Wooley Two's compliment Signed numbers: Baugh-Wooley Two's compliment Signed multipliers is the best known algorithm for signed multiplication because it maximizes the regularity of the multiplier and allow all the partial products to have positive sign bits[3].Baugh–Wooley technique was developed to design direct multipliers for Two's compliment numbers [9].When multiplying two's compliment numbers directly, each of the partial products to be added is a signed numbers. Thus each partial product has to be sign extended to the width of the final product in order to form a correct sum by the Carry Save Adder (CSA) tree. According to Baugh-Wooleyapproach, an efficient method of adding extra entries to the bit matrix suggested to avoid having deal with the negatively weighted bits in the partial product matrix. In fig1 (a) & (b)partial product arrays of 5*5 bits Unsigned and Signed bits are shown:

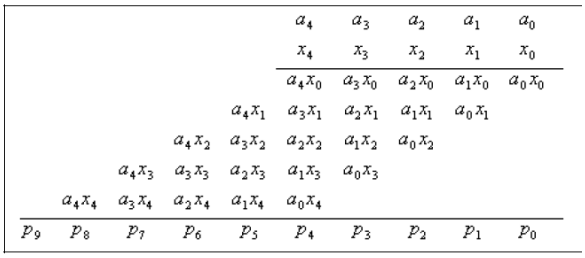


FIG1 (a): 5*5 unsignedmultiplications

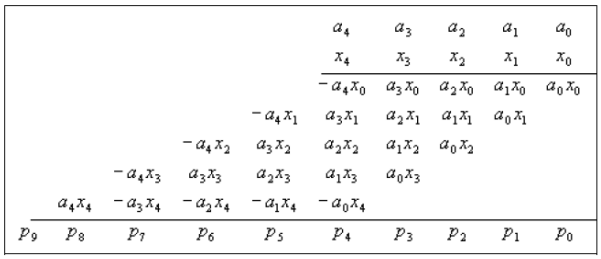


FIG1 (b): 5*5 Signed Multiplication

Figure 1 (c) shows how this algorithm works inthe case of a 5x5 multiplication. The first three rows are referred to as PM (partial *products withmagnitude part*) and generated by one NAND and three AND operations. The fourth row is called as PS (*partial products with sign bit*) and generated by one AND andthree NAND operations with a sign bit. Consider the partialproducts of PM. Suppose $b_2 = b_0$in figure1 (c). Then the third row can be obtained by shifting the first rowby 2 bits. Likewise, shift operation can be used to obtain a partial product of different bit level as in sign magnitude multiplication.

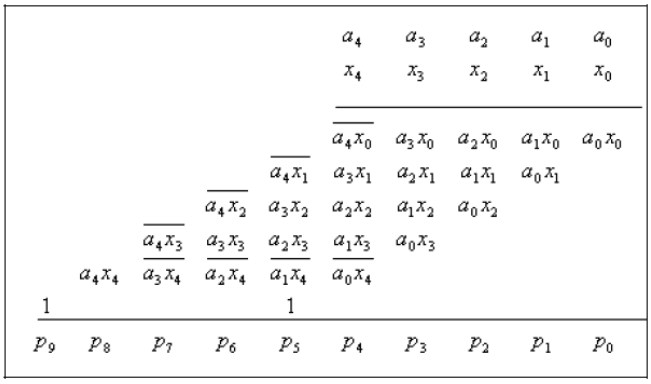


FIG1 (c): 5*5 Multiplication Example of Baugh-WooleyArchitecture

Baugh-Wooley schemes becomean area consuming when operands are greater than or equal to 32 bits. The rest of the paper is organised as follows. The baugh-Wooley architecture is explained in section 2. Implementation results in terms of power, area, and speed 4 bit multipliers and comparison are presented.

2 Baugh-Wooley Architecture

Hardware architecture for Baugh-Wooleymultiplier is shown in fig 2.It follows left shift

algorithm. Through mux we can select which bitwill multiply.

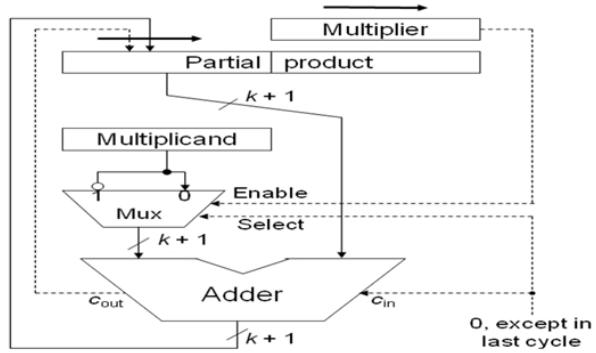


Fig 2: Signed 2's-Complement Baugh-Wooley Hardware Multiplier

Suppose we are adding +5 and -5 in decimal we get '0'. Now, represent these numbers in 2's complement form, and then we get +5 as 0101 and -5 as 1011. On adding these two numbers we get 10000. Discard carry, then the number is represented as '0'.

Baugh-WooleyMultiplier [5]:

Baugh-Wooley Multiplier is used for both unsigned and signed number multiplication. Signed Number operands which are represented in 2's complemented form. Partial Products are adjusted such that negative sign move to last step, which in turn maximize the regularity of the multiplication array. Baugh-Wooley Multiplier operates on signed operands with 2's complement representation to make sure that the signs of all partial products are positive.

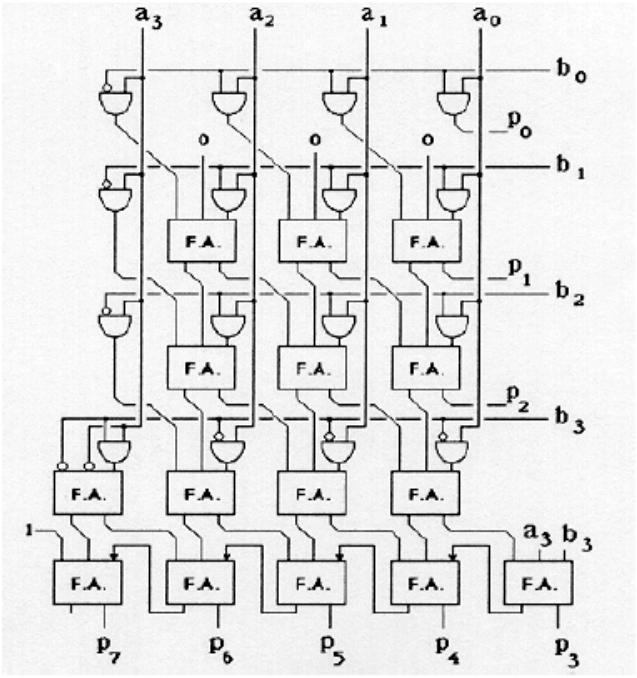


Fig 2: Block diagram of a 4*4 Baugh-Wooley multiplier

Here are using fewer steps and also lesser adders. Here a0, a1, a2, a3& b0, b1, b2, b3 are the inputs. I am getting the outputs that are p0, p1... p7. As I am using pipelining resister in this architecture ,so it will take less time to multiply large number of 2's compliment but less than 32 bit .Above 32 bit Modified Baugh-Wooley Multiplier is used.

Multiplier Architecture	Number of LUTS	Fan out	Clock-Period (ns)	Power Dissipation (mw)
Add-and-Shift	74	18	8.939	68.89
Baugh-Wooley	32	104	15.029	67.84

Table 1: Synthesis results of different 4-bit pipelined multiplier architectures

Multiplier Architecture	Number of LUTS	Fan out	Clock-Period (ns)	Power Dissipation (mw)
Add-and-Shift	74	18	8.939	68.89
Baugh-Wooley	30	46	3.921	15.3

Table 2: My Synthesis results of different 4-bit pipelined multiplier architectures

3 Implementation Results and Comparisons

In this study, I use 4-bit pipelined multipliers and are implemented in VHDL and logic simulation is done by using ModelSim Designer and the synthesis is done using Xilinx ISE 8.2i of Device 4VFX20FF672-12.The synthesis result of 4-bit pipelined Baugh-Wooley architecture is shown in table above of the reference paper and my paper.

In my paper I amusing Brent-Kung adder (BK adder), an advanced design prefixadder, which is a very good balance between area and power cost and also it will present better performance. This adder has a complex carry and inverse carry tree . A tree can be divided into 2 types that is a tree and an inverse tree. The upper tree based on periodic power of 2. The inverse tree is offset 1, beginning from the bottom of the matrix and expanding outwards at powers of 2.

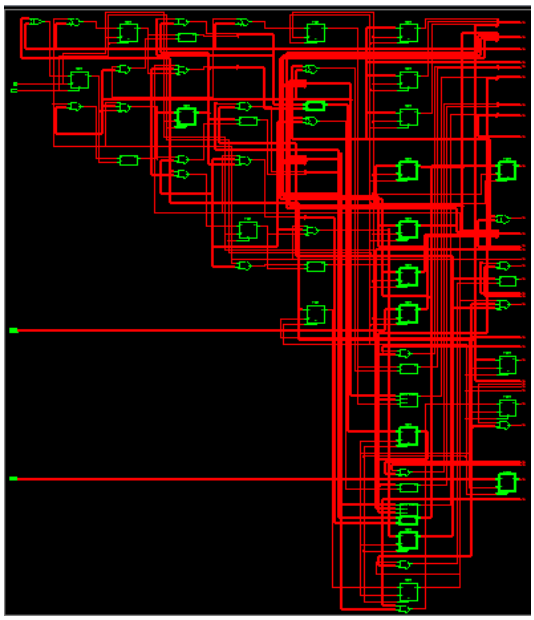


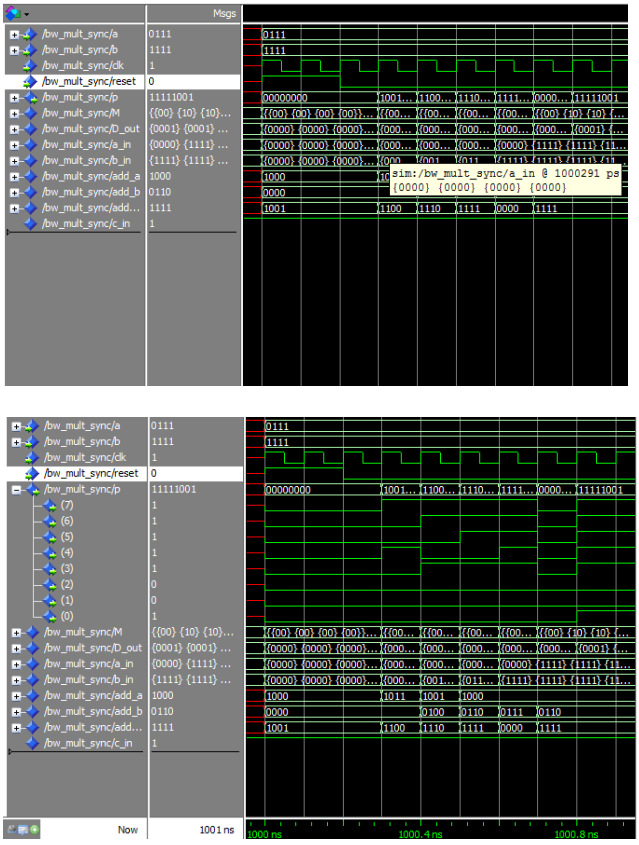
Fig 3: Synthesis Report of Baugh-Wooley Architecture

The results show that the Baugh-Wooley multiplierhas increased speed since clock period isonly15.861ns. Pipeline stages further improve theBaugh - Wooley architecture speed. Number of LUTs represents the area required for implementation.

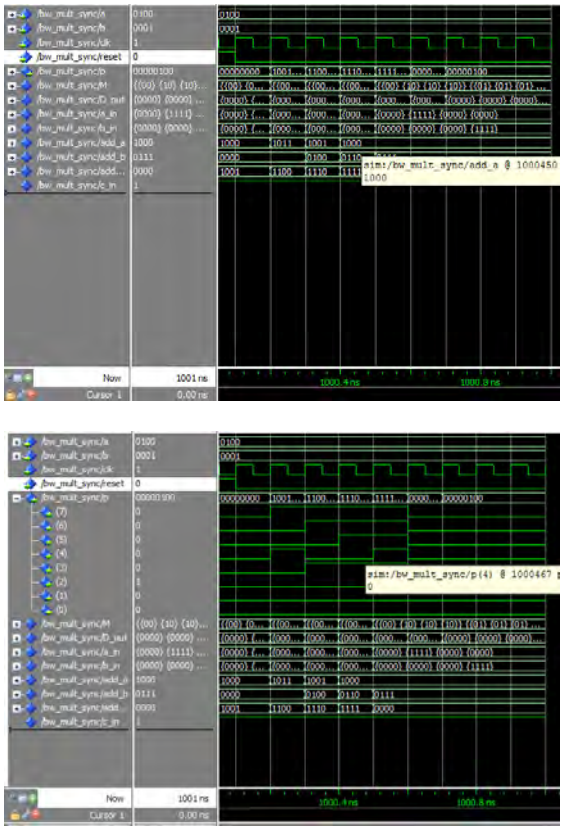
Thenumber ofLUTsrequiredin Baugh-Wooley architecture is 30 compared to 32. The fan-out of the multiplier architectureis also given which directly gives the possibility of the multiplier to form large circuits. This can be extended to the pipelined multiplier architecture also to verify the parameters. Latency and speed are the

important factors with pipelining under consideration. The synthesis results of 4-bit pipelined multipliers are shown in Table 2.Power consumption in Baugh-Wooley multipliers isminimum compared to other conventionalmultiplier units. So it clears that the signed binary multiplicationthrough Baugh-Wooleymultiplication is suited for large multiplier implementation. Theimprovements in constraint can be used to make Baugh-Wooley multiplier more efficient .The fan-out of the multiplier architecturesare also given which directly gives the possibility of themultiplier to form large circuits. This can be extended tothe pipelined multiplier architecture also to verify theparameters. Latency and speed are the important factors with pipelining under consideration. The synthesis resultsof 4-bitpipelined multipliers are shown in Table 2. Thepipeline constraint increases the speed of the multiplier considerably with a increase in powerconsumption. For the Baugh-Wooley multipliers, the clock period reduces to 3.321ns as a result of pipelineregisters implemented. This improves the speed whichmay reduce due to the BK adder which I used in my architecture. The maximum delay for this architecture is 2.143ns.i am using 65 Flip Flop out of 17088 and maximum frequency is 527.037MHZ which is a good sign .The incorporation of the pipeline multipliers thus canbe effectively done to make the chip efficientlyreconfigurable among the two reconfiguration modes andthis work is in progress. The possibility of other reconfiguration constraints is under work and theimplementation of the reconfiguration modes accordingto these constraints are the future work.

Output Simulation Result For
Baugh- Wooley Architecture:



Simulation Result For Both Unsigned Numbers Multiplication



Simulation Result For Unsigned and Signed Number Multiplication

4 Conclusion

An efficient multiplier todeal with the latency problemis proposed. This paperpresents acomparison between various multiplierarchitectures with area, speed and power as the mainconstraints. It is observed that the Baugh-Wooleyarchitecturegives optimized values for variousconstraints andhence suited for long bitmultiplication up to less than 32 bit. The pipelining resister techniques are used to improve themultiplier characteristics.

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